A Method for Legalizing the Placement of Cells in an Integrated Circuit Layout

Abstract of the Disclosure

A method for resolving overlaps in the cell placement (placement legalization) during the physical design phase of an integrated chip design is described. This problem arises in several contexts within the physical design automation area including global and detailed placement, physical synthesis, and ECO (Engineering Change Order) mode for timing/design closure The method involves capturing a view of a given placement, solving a global two-dimensional area migration model and locally perturbing the cells to resolve the overlaps with minimal changes to the given placement. The method first captures a two-dimensional view of the placement including blockage-space, free-space and the given location of cells by defining physical regions. The desired global area migration across the physical regions of the placement image is determined such that it satisfies area capacity-demand constraints. The method also provides moving the cells between physical regions along previously computed directions of migration to minimize the movement cost. Also provided is an approximate method to model the movement of multi-row high cells.